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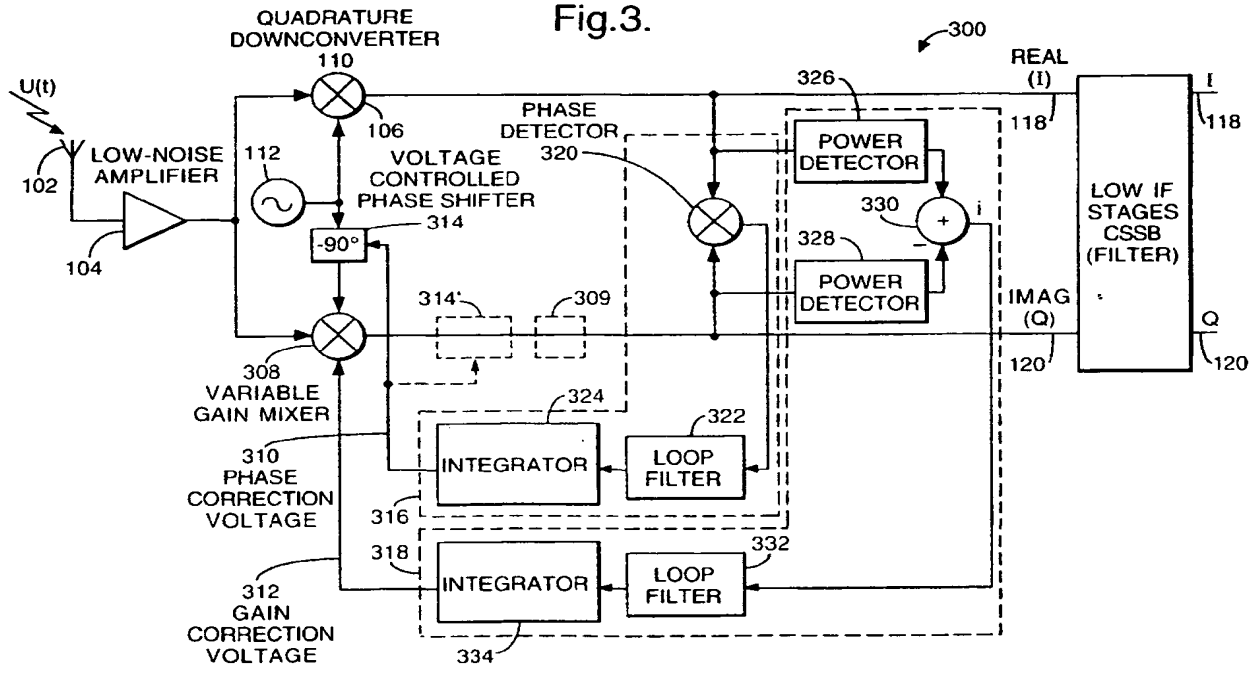
(54) Radio receiver and method of operation

(57) A phase compensation loop suitable for a quadrature receiver comprises a phase comparator having in-phase and quadrature signals fed to respective inputs of the phase comparator. The phase comparator outputs a signal which represents a deviation from mutual phase quadrature of the in-phase and quadrature signals input to the comparator. The signal output from the phase comparator is input to a controllable phase shifter which shifts the phase of the in-phase or quadrature signal in accordance with the signal from the phase comparator to bring them into mutual phase quadrature.

Fig.3.



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Description

The present invention relates to a radio receiver, in particular but not exclusively, to a phase compensation loop for a quadrature receiver.

The current trend in receiver technology is to reduce weight, volume, power consumption and cost. This is particularly important for receivers in portable apparatus such as radio telephones. This has resulted in receiver architecture designs in which there are no or few discrete radio frequency (RF) and intermediate frequency (IF) filters in the receiver front end.

An example of a receiver architecture having few discrete RF and IF filters is a single conversion low-IF architecture for a quadrature receiver. Single conversion low-IF architectures typically produce an image signal which is very close to the wanted signal. Such image signals are termed "in-band" image signals, and may be filtered out using a single sideband filter. However, a portion of the image signal appears at the wanted signal frequency as cross-talk if there is an imbalance between the phase and/or gain of respective quadrature signals. It is desirable for such cross-talk to be reduced or rejected. Typically, a quadrature receiver front end can only achieve about 30dB of image-to-signal cross-talk rejection, which is often insufficient for many applications such as radio telephones.

A solution to the problem of cross-talk is to use a double-quadrature mixer architecture. However, such an architecture requires 90° phase shifts on both the local oscillator and RF ports coupled to four mixers. Providing at least one of the ports (e.g. the local oscillator) is phase and amplitude balanced, any imbalance at the other port (e.g. the RF port) results in a spurious product at a frequency given by the sum of the RF and local oscillator frequencies. This can be easily filtered out using an RF bandpass filter before the mixers.

A drawback of the above approach is that four mixers are required resulting in relatively high power consumption. Additionally, a relatively bulky RF 90° hybrid coupler is also required together with quadrature balance on the local oscillator port.

According to a first aspect of the invention there is provided a phase compensation loop for a quadrature receiver adapted to generate first and second quadrature signals from a received signal, the phase compensation loop comprising : a phase comparator for receiving the first and second signals and adapted to output a third signal indicative of deviation from mutual phase quadrature of the first and second signals; and phase shifting means for shifting the phase of the first signal in accordance with the third signal thereby bringing the first and second signals towards mutual phase quadrature.

According to a second aspect of the invention there is provided a method for phase compensation in a quadrature receiver adapted to generate first and second quadrature signals from a received signal, the method comprising the steps of: comparing the phase of the first signal with the phase of the second signal; deriving a third signal indicative of deviation from mutual phase quadrature of the first and second signals, and shifting the phase of the first signal in accordance with the third signal.

Preferred embodiments in accordance with first and second aspects of the invention have the advantage that the first and second signals may be brought towards mutual phase quadrature by appropriate control of the phase shifting means. Thereby image cross-talk may be reduced. This obviates the need for image rejection filters in the RF front end of the receiver which results in lower weight, volume, loss and cost for such receivers.

In a preferred embodiment the phase shifting means is disposed in the radio frequency front end of a quadrature receiver which has the advantage that any image rejecting filters in the intermediate frequency region of the receiver are less likely to be overdriven by a strong image signal.

Preferably, the phase shifting means comprises a transistor or varactor diode, which provides for fine phase adjustment for high image rejection.

Optionally, the phase shifting means is disposed after the radio frequency front end and is operable for signals at an intermediate frequency of a quadrature receiver. Such an intermediate frequency may be zero Hertz (0Hz) for a phase compensation loop disposed in a direct conversion receiver, for example.

Suitably, the phase shifting means and/or phase comparator comprise an appropriately conditioned digital signal processor, which advantageously is environmentally independent and does not require external integrator or filter components. Alternatively, the phase shifting means comprises an analogue all-pass filter.

The phase compensation loop may comprise a loop filter having an input for receiving the third signal and an output for providing a control signal to the phase shifting means, thereby providing for tracking a dynamic phase imbalance between first and second signals.

Embodiments in accordance with the invention will now be described, by way of example only, and with reference to the accompanying drawings, in which:

Figure 1 is a schematic diagram of a quadrature single-conversion RF front end;

Figure 2 shows a schematic representation of wanted and image signals, and image crosstalk;

Figure 3 is a schematic diagram of a quadrature receiver in accordance with an embodiment of the present inven-

tion:

Figure 4A is a schematic diagram of a conventional phase locked loop;

Figure 4B is a schematic diagram of a phase compensation loop in accordance with an embodiment of the present invention: and

Figure 5 is a schematic diagram of a gain compensation loop.

Figure 1 shows a schematic diagram for a quadrature single-conversion receiver RF front end 100. A radio frequency signal v(t), such as an AM or FM modulated signal, is received by antenna 102. The received signal v(t) is amplified by low-noise amplifier 104 and the amplified signal is input to mixers 106 and 108 by a power splitter. The mixers 106 and 108 form part of quadrature down-converter 110. The signal LO output from local oscillator 112 has a frequency which is very close to the carrier frequency, fc, of the received_signal v(t). The LO signal is fed directly into mixer 106 and is fed into mixer 108 via a - 90° phase shifter 114. Optionally, mixers 106 and 108 could each be fed via phase shifters.

Respective signals output from mixers 106 and 108 have a centre frequency at an intermediate frequency, I_F. For a single conversion receiver suitable for a radio telephone the IF may be as low as half of the signal bandwidth which is close to the baseband frequency of a typical radio telephone. This would be 20kHz for a radio telephone operating in an analogue radio telephone system such as Total Access Communication System (TACS), or 100kHz for the Global System for Mobiles (GSM) radio telephone system. The IF signal from mixer 106 is referred to as the "Real" or "in-phase" (I) signal, and the IF signal from mixer 108 is termed the "Imaginary" or "Quadrature" (Q) signal.

Both the I and Q IF signals, hereinafter referred to as I and Q signals, comprise a wanted signal and image signal as shown in Figure 2 using the I signal as an example. The origin of image signal 202 and wanted signal 204 is well known to persons of ordinary skill in the art, and will not be discussed further.

Figure 2 shows responses at the wanted frequency ω_{IF}, and an unwanted image response at $-\omega_{IF}$. The response at ω_{IF} comprises the wanted signal 204 and an unwanted interfering signal 208. Unwanted signal 208 is a fraction of an image signal 202 occurring at a frequency $-\omega_{IF}$ and is known as an image cross-talk signal. Signal 206 is a fraction of the wanted signal 204, and interferes with image signal 202.

Cross-talk signals may arise due to phase and/or gain imbalance between mixers 106 and 108. In practical systems this is a serious drawback since pairs of mixers which are sufficiently well-balanced to reduce cross-talk to - 60dB for example, as required by operating standards for cellular telephones, are commercially unavailable. Other sources of phase/gain imbalance may be temperature variations or varying input loads on the mixers for example.

A first embodiment of a quadrature single-conversion receiver 300 in accordance with the present invention is shown in Figure 3. Like elements to those shown in Figure 2 are referred to with like reference numerals.

Radio frequency signal v(t) is received by antenna 102 and amplified by low-noise amplifier 104. The amplified output from low-noise amplifier 104 is then input to quadrature down converter 110, which provides means for generating quadrature signals from receiver signal v(t). The low-noise amplifier 104 and quadrature down converter 110 form a RF front end for receiver 300, which converts the received RF signal v(t) down to a frequency $+\omega_{IF}$ and an image signal to a frequency - ω_{IF} for the RF signal v(t) having a greater frequency than a local oscillator signal (LO) and the image signal having a lower frequency than the local oscillator signal (LO) . Quadrature down converter 110 comprises mixers 106 and 308. Mixer 106 is driven directly by the output (LO) of local oscillator 112. Mixer 308 is a variable gain mixer, and is driven by the output (LO) of local oscillator 112 having passed via phase shifting means such as voltage controlled phase shifter 314. The voltage controlled phase shifter 314 provides a nominal phase shift of -90°. Voltage controlled phase shifter 314 is controlled by phase correction voltage 310 originating from phase correction loop 316, and the variable gain mixer 308 is controlled by the gain correction voltage 312 derived from the gain correction loop 318. Alternatively, a voltage controlled phase shifter 314' may be provided to act on the Q signal output from mixer 308, and phase shifter 314 may be static at a nominal -90°. The low IF stage comprises a Single Side Band (SSB) filter 116 which passes the wanted signal at $+\omega_{IF}$ and attenuates the image signal at $-\omega_{IF}$. The real and imaginary outputs 118/120 respectively are provided to a complex domain demodulator, for example a FM detector or a digital detector suitable for digital systems. Optionally, mixer 308 may be a static gain mixer, and an extra gain element 309 may be provided on the output of mixer 308.

Phase correction is performed using phase correction loop 316 which is a modified form of a phased lock loop (PLL). Phase detector 320 has the I and Q signals respectively generated by mixers 106 and 308 input to it and generates an output which is proportional to a deviation from 90° in the phase difference between the I and Q signals. If the difference between the I and Q signals is exactly 90°, then the output of phase detector 320 is zero. The output of phase detector 320 is input to an optional phase loop filter 322. Phase loop filter 322 is not required if the phase imbalance does not change, or varying imbalance phase does not need to be tracked. The output from phase loop filter 322 is forwarded to integrator 324. Integrator 324 integrates the phase detector output and generates a phase correction voltage which may be applied to phase shifter 314. The phase correction loop adjusts the voltage control to phase shifter 314 until the phase difference between the I and Q signals is exactly 90°. Phase shifter 314 may

comprise any suitable phase shifting means such as a transistor or varactor diode, whereby phase control may be achieved by varying the current flowing through the transistor or voltage across varactor diode. If there are any DC offsets in any of the components comprising the phase correction loop then these will either have to be calibrated out on initialising the system, or taken into account when controlling the voltage controlled phase shifter 314.

Gain correction is performed by gain correction loop 318, which comprises power detectors 326 and 328 respectively. Signals I and Q are input respectively to power detectors 326 and 328. The outputs from respective power detectors 326/328 are input into subtractor 330. The output from subtractor 330 is input to optional gain loop filter 332. Gain loop filter 332 is not required if the gain imbalance does not change, or varying gain imbalance does not need to be tracked.

The power detectors 326 and 328 generate outputs proportional to the I and Q signal powers respectively. When the gain in each path is the same, the output from subtractor, typically a differential amplifier, is zero.

The output from gain loop filter 332 is fed into integrator 334 which outputs a gain correction voltage 312 to variable gain mixer 308. Utilising the above described gain correction loop, gain imbalance between the I and Q signals may be reduced.

A quadrature single-conversion receiver in accordance with the circuit shown schematically in Figure 3 is capable of providing I and Q signals comprising low levels of cross-talk. A more detailed description of the operation of the phase correction loop will now be described, with reference to Figure 4.

Figure 4A shows a typical phase locked loop (PLL). Phase detector 402 has an output *p(t)* which is proportional to the difference in phase between reference signal *i(t)* and the Voltage Controlled Oscillator (VCO) 406 output signal *q(t)*. The output signal *p(t)* for phase detector 402 is input to a loop filter 408. Loop filter 408 has a transfer function given by *H(s)*. The output *y(t)* from loop filter 408 is fed into the input of VCO 406. Phase detector 402 has a gain of Kp in units of volts per radian, and VCO 406 has a gain of Kv in units of radians per second per volt. For a digital phase comparator, for example an XOR gate, and where *i(t), q(t)* are digital wave forms, the phase detector characteristic is linear. When an analogue multiplier type of phase detector is used the output *p(t)* is proportional to sin (θ), where θ is the phase difference between the input_signals. The output of phase detector 402 is zero when the phase difference between the inputs is 90° or -90°. A PLL of this type therefore locks its VCO to the same frequency as, but 90° out of phase with, the reference frequency.

The phase correction loop in accordance with the embodiment shown in Figure 3 acts to provide a 90° phase difference between the I and Q signal in the quadrature single-conversion receiver. By replacing the VCO shown in Figure 4A above with an imaginary signal Q, and the reference signal *i(t)* by the real signal I it is possible to provide a 90° phase difference between the I and Q signals. Effectively, the VCO is replaced by the Q signals front end mixer 308, phase shifter 314 and all its IF processing circuitry from Figure 3. The Q signal is now phase controlled, and can be varied independently of the local oscillator drive in order to achieve an appropriate phase balance. A schematic diagram of such a system suitable for the alternative embodiment of receiver 300 described above is described below with reference to Figure 4B.

The phase correction loop schematically shown in Figure 4B, is described in the frequency (s) domain. A signal X(s) is input to RF front end mixers 410. The I channel output $\theta_i(s)$ is input to a phase comparator 412. The quadrature output is fed into phase shifter 414 and the resulting quadrature signal $\theta_q(s)$ is fed into the negative input of comparator 412. For simplicity, an ideal phase comparator function $\theta_{ew} = \theta_i(s)-\theta_q(s)$ is assumed, where θ_{ew} is the phase difference. A skilled person would readily appreciate that any offsets or non-linearities in phase comparator 412 would have to be accounted for during calibration of the comparator. The output of comparator 412 goes to gain element 416 which has a gain of Kc. Gain element 416 represents the gain associated with the phase detector. The output from gain element 416 is input to a loop filter 418 having a transfer function H(s). The output from the loop filter 418 is input to an integrator 420 having a transfer function 1/s. The output from the integrator $V_f(s)$ is input to phase shifter 414. Phase shifter 414 has a gain K_f with dimensions of radians per volt. The output of the loop is given as $V_0(s)$.

The phase correction loop transfer function is given by;

$$\frac{V_0(s)}{\theta_i(s)} = \frac{k_c s H(s)}{s + k_c k_f H(s)} \tag{4}$$

For a first order PLL in which H(s)=1;

$$\frac{V_0(s)}{\theta_i(s)} = \frac{k_c s}{s + k_c k_f} \tag{5}$$

The response to a unit impulse in phase is given by $\theta_i(s)=1$,

such that

$$V_0(s) = \frac{k_c s}{s+k_c k_f}, \quad (6)$$

and
the response to a step change in phase is given by $\theta_i(s)=1/s$.
such that

$$V_0(s) = \frac{k_c}{s+k_c k_f}. \quad (7)$$

The inverse Laplace transform produces,

$$v_0(t) = k_c e^{kckft} \quad (8)$$

for the time domain.

Equation (8) describes the transient response of the loop to a step change in θ_i channel phase error. For t tending to infinity;

$$v_0(\infty) = k_c e^{-\infty} = 0. \quad (9)$$

The phase error $\varepsilon(s)$ is proportional to $V_0(s)$ when $H(s)=1$;

$$\varepsilon(s) = \frac{V_0(s)}{k_c H(s)} \xrightarrow{H(s)=1} \frac{V_0(s)}{k_c}, \quad (10)$$

and in time, the final phase error

$$\varepsilon(\infty)=0. \quad (11)$$

Thus, a modified first order phase locked loop can be used for I/Q phase balance correction. However, a second order loop is required in order to track a changing phase imbalance ($H(s)\neq 1$). Such a second order loop will be readily implementable by a skilled person.

The loop gain $k_f k_c$ determines the dynamic properties of the loop. Reducing the gain narrows the bandwidth, raising the gain increases the bandwidth. The problem with too large a bandwidth is that phase noise (i.e. the quadrature component of the system noise) will start to take an effect on the loop. In many applications the time taken for the receiver to settle is important. If the loop bandwidth is too narrow, the image rejection will not settle quickly enough. Providing the integrator holds its voltage, the image rejection will be maintained between typical Time Domain Multiplex (TDM) receive bursts for example in a radio telephone system.

The operation of the optional embodiment of gain compensation loop 318 comprising a gain element 309 provided at the output of mixer 308 shown dotted in Figure 3 will now be described with reference to Figure 5.

The gain loop shown in Figure 5 may be utilised to correct or reduce gain imbalance in the front end mixers of a quadrature receiver such as shown in Figure 3. The gain compensation loop is similar in operation to the phase compensation loop described above except that the phase shifter is replaced with a gain controller and power is measured instead of phase. The power measurement is made by squaring or rectifying, and smoothing the outputs from the I and Q channels.

Mathematically, the operation of the gain compensation loop may be described using equations (4) through to (11) with signal power P_i and P_q substituted for signal phase θ_i, θ_q.

The gain compensation loop shown schematically in Figure 5 will now be described with reference to the frequency

domain. The I channel output $P_i(s)$ is input to a gain comparator 504. The Q channel output $P_q(s)$ is input to a gain control element 506, and the output from the gain control element 506, is fed into the negative input of gain comparator 504. The output of gain comparator 504 is fed to gain element 508 having a gain k_c' and which represents the gain associated with the gain comparator 504. It will be evident to a skilled person that gain element 508 need not exist in practice.

The output of gain element 508 is input to gain loop filter 510 which has a transfer function H(s) and provides an output signal Vo(s). Signal Vo(s) is integrated by integrator 512 having a transfer function 1/s, and provides output signal Vf(s) to gain controller 506. Gain controller 506 has a gain k_f with dimensions of decibels per volt. Optionally, the gain control could be dimension less and be the ratio of output to input voltage.

The gain correction loop transfer function is given by

$$\frac{V_0(s)}{P_i(s)} = \frac{k_c s H(s)}{s+k_c k_f H(s)} \tag{12}$$

For a first order gain correction loop in which H(s)=1:

$$\frac{V_0(s)}{P_i(s)} = \frac{k_c s}{s+k_c k_f} \tag{13}$$

The response to a unit impulse in gain is given by $P_i(s) = 1$ yielding

$$V_0(s) = \frac{k_c s}{s+k_c k_f}, \tag{14}$$

and
the response to a step change in gain is given by $P_i(s) = 1/s$, yielding

$$V_0(s) = \frac{k_c}{s+k_c k_f} \tag{15}$$

Taking the inverse Laplace transform of (15) yields

$$V_0(t) = k_c e^{k_c k_f t} \tag{16}$$

for the time domain, and describes the transient response of the gain compensation loop to a step change in I channel gain error.

For t tending to infinity

$$V_0(\infty) = k_c e^{-\infty} = 0 \tag{17}$$

The gain error E(s) is proportional to $V_0(s)$ when H(s) = 1, yielding

$$E(s) = \frac{V_0(s)}{k_c H(s)} \xrightarrow{H(s)=1} \frac{V_0(s)}{k_c} \tag{18}$$

and in time the final gain error

$$E(\infty)=0.$$

Thus, a first order gain locked loop can be used for I/Q gain balance correction in a similar manner to phase locked loop described above. Similarly, a second order loop is necessary to track a dynamic gain imbalance.

In similar fashion as for the phase compensation loop described above, the loop gain $k_c k_f$ determines the dynamic properties of the gain compensation loop. Reducing the gain narrows the bandwidth, raising the gain increases the bandwidth.

The embodiments of the phase compensation loop and gain compensation loop respectively described with reference to Figures 4B and 5, show the phase shifter 414 and gain controller 506 located after the RF front end mixers. Optionally, the phase shifter and gain controller may be incorporated in the RF front end as phase shifter 314 and variable gain mixer 30 thereby forming part of quadrature down converter 110 shown in Figure 3.

The phase detector/comparator 320,412 and power detector/comparator 326,504 may be implemented digitally using digital signal processing (DSP) techniques based on the same mathematical principles described above. For example, a controllable phase shifter may be implemented by a Hilbert Rotator or by utilising the well-known CORDIC algorithm ("YU HEWHU CORDIC-Base VLSI Architectures for Digital Signal Processing" IEEE Signal Processing Magazine, July 1992).

In view of the foregoing description it will be evident to a person skilled in the art that various modifications may be made within the scope of the invention.

The scope of the present disclosure includes any novel feature or combination of features disclosed therein either explicitly or implicitly or any generalisation thereof irrespective of whether or not it relates to the claimed invention or mitigates any or all of the problems addressed by the present invention. The applicant hereby gives notice that new claims may be formulated to such features during prosecution of this application or of any such further application derived therefrom.

Claims

1. A phase compensation loop for a quadrature receiver adapted to generate first and second quadrature signals from a received signal, the phase compensation loop comprising:

   a phase comparator for receiving the first and second signals and adapted to output a third signal indicative of deviation from mutual phase quadrature of the first and second signals; and
   phase shifting means for shifting the phase of the first signal in accordance with the third signal thereby bringing the first and second signals towards mutual phase quadrature.

2. A phase compensation loop according to claim 1, wherein the phase shifting means comprises a transistor, or a varactor diode.

3. A phase compensation loop according to claim 1 or claim 2, wherein the phase shifting means is operable for signals at an intermediate frequency of the quadrature receiver.

4. A phase compensation loop according to claim 3, wherein the phase shifting means and/or phase comparator comprise a suitably conditioned digital signal processor.

5. A phase compensation loop according to claim 1, wherein the phase shifting means comprises an analogue all-pass filter.

6. A phase compensation loop according to any preceding claim, further comprising a loop filter having an input for receiving the first signal and output for providing a control signal to the phase shifting means.

7. A method for phase compensation in a quadrature receiver adapted to generate first and second quadrature signals from a received signal, the method comprising the steps of:

   comparing the phase of the first signal with the phase of the second signal;
   deriving a third signal indicative of deviation from mutual phase quadrature of the first and second signals, and
   shifting the phase of the first signal in accordance with the third signal.

8. A quadrature receiver, comprising a phase compensation loop according to any preceding claim.

9. A quadrature receiver according to claim 8, wherein the phase shifting means is disposed in the radio frequency

front end of the quadrature receiver.

Fig.1.

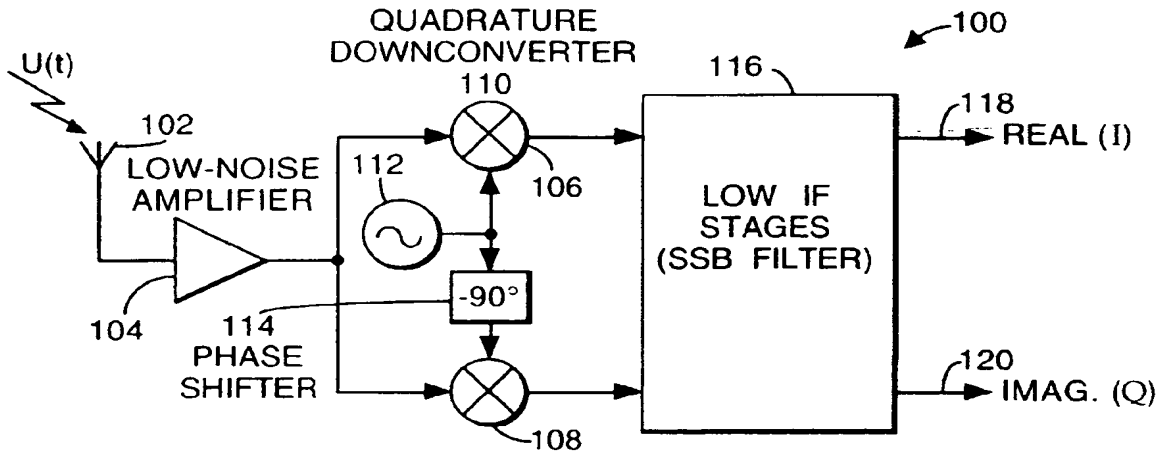
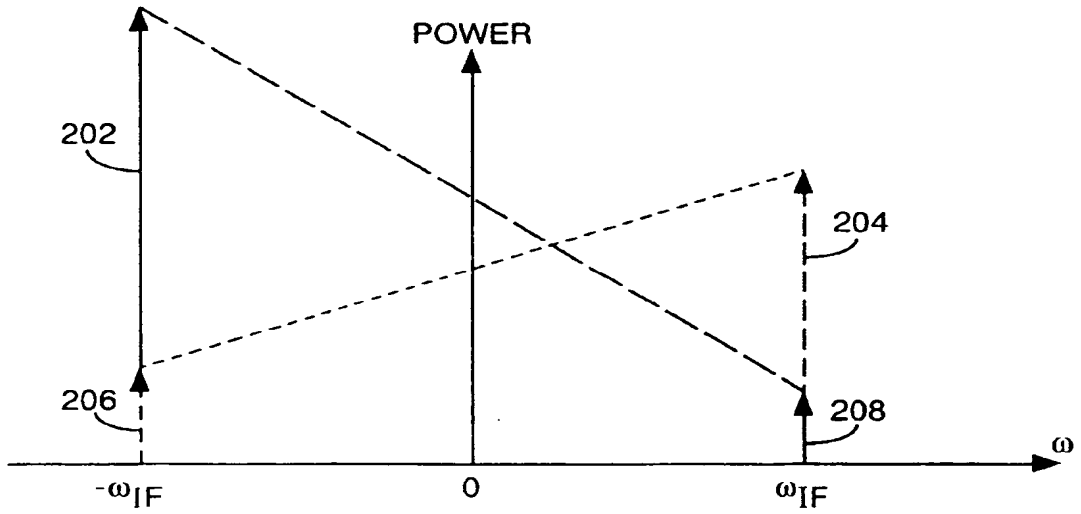


Fig.2.



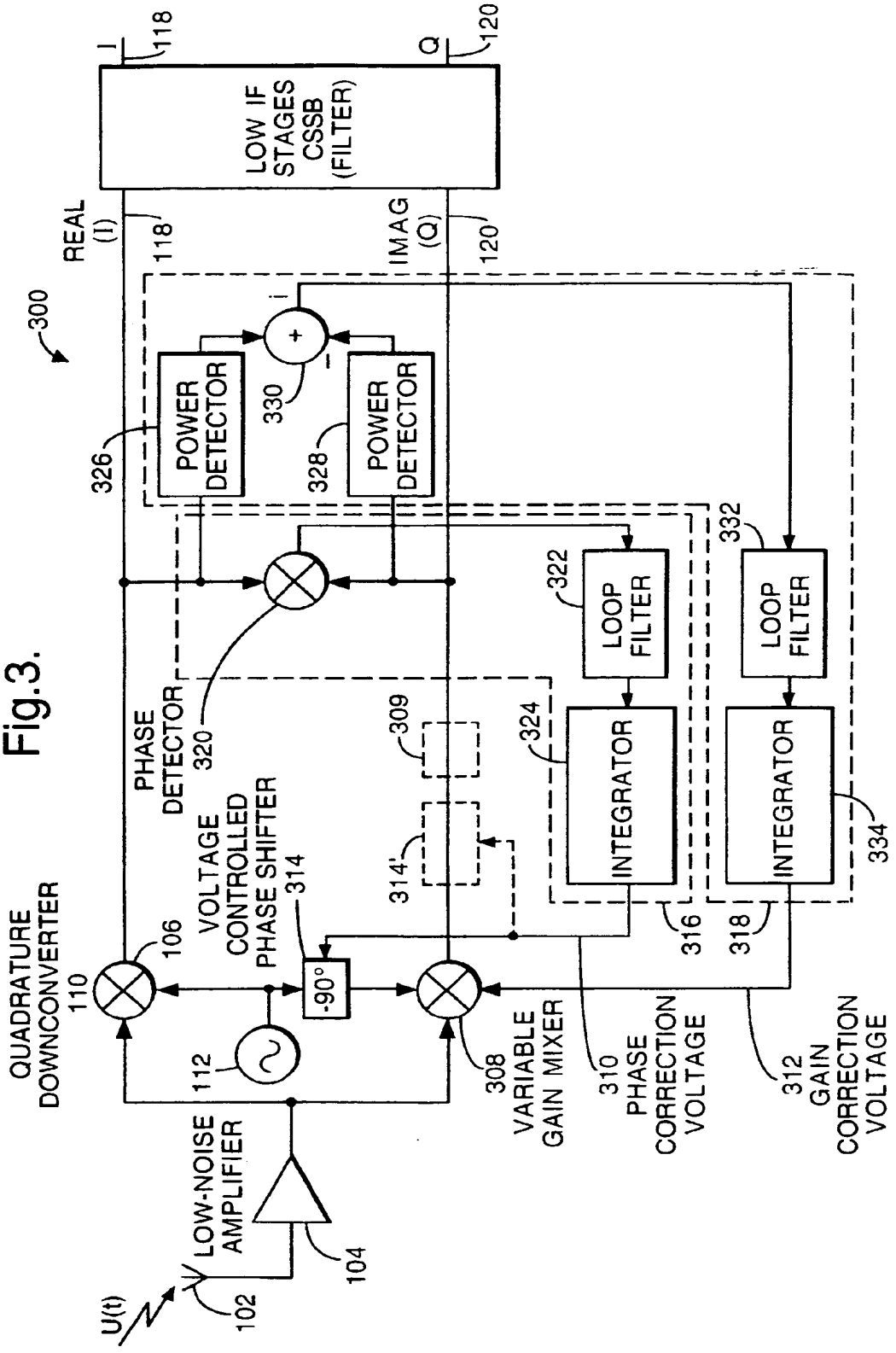


Fig.3.

Fig.4A.

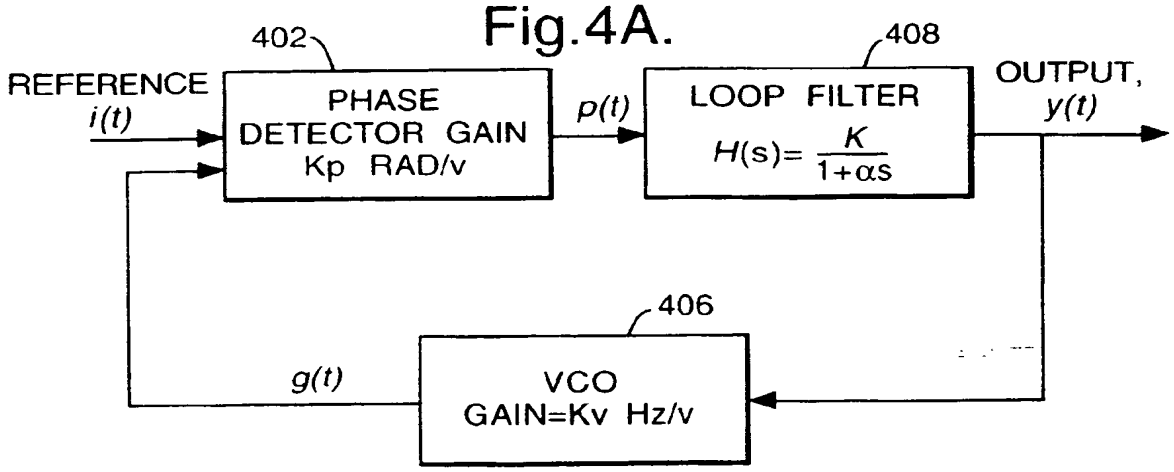


Fig.4B.

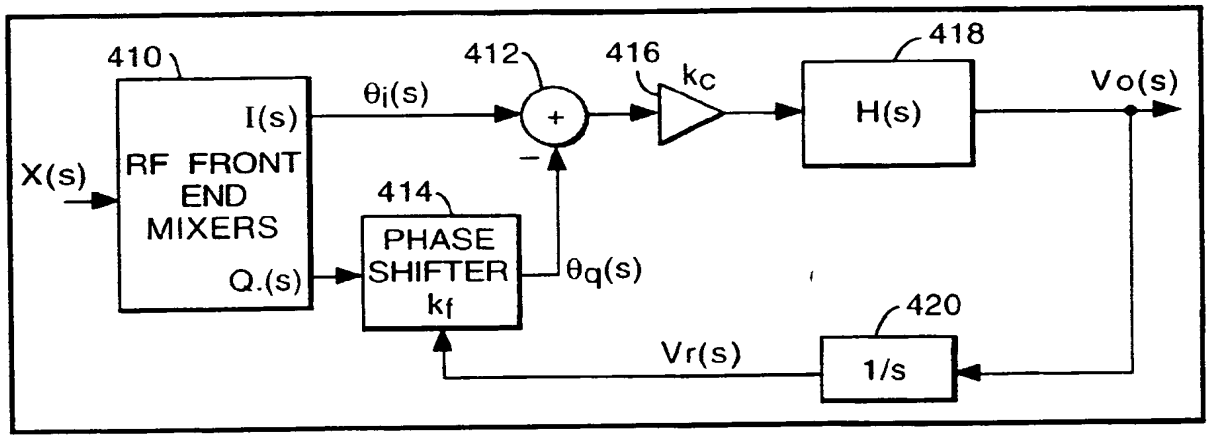
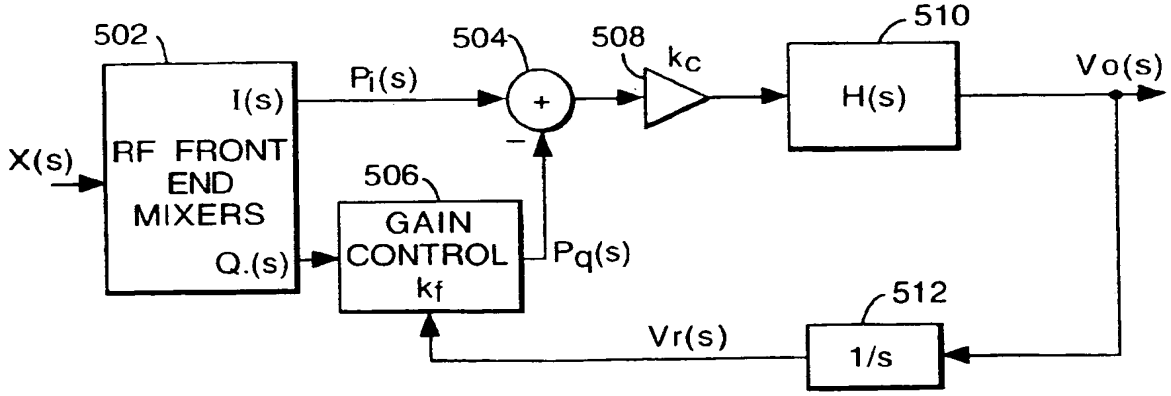


Fig.5.



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EUROPEAN SEARCH REPORT

Application Number
EP 98 30 4283

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X Y	GB 2 296 613 A (UNIV BRISTOL) 3 July 1996 * page 7, line 16 - page 8, line 35; figure 2 *	1,3,6,7, 9,10 2,5	H03D3/00 H03D7/18
Y	EP 0 455 156 A (SIEMENS AG OESTERREICH ;SIEMENS AG (DE)) 6 November 1991 * figures 1,2 *	2	
Y	US 3 969 682 A (ROSSUM DAVID PHILIP) 13 July 1976 * abstract *	5	
A	US 3 748 572 A (KIM K ET AL) 24 July 1973 * column 3, line 15 - line 26 *	1,2,7	
A	EP 0 678 976 A (BRITISH TECH GROUP) 25 October 1995 * abstract, last line *	4	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

H03D
H03H

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	4 September 1998	Peeters, M

CATEGORY OF CITED DOCUMENTS

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